SIGNETICS

DCL

INTEGRATED CIRCUITS

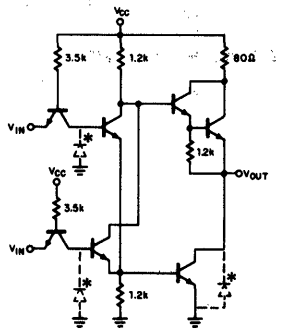
8815 DUAL 4-INPUT NOR GATE
8875 TRIPLE 3-INPUT NOR GATE
8885 QUAD 2-INPUT NOR GATE

The 8815, 8875 and 8885 gates perform the logic NOR function for positive logic (the logic "ONE" is assigned to the highest voltage level) and complement the NAND gate elements 8816, 8870 and 8880.

These gates are all designed for high speed application while maintaining high fan-out and noise margin.

The parallel transistor structure forms the NOR function. All unused inputs must be tied to ground. The output arrangement is basically the same as the NAND implementation providing low impedance for both logic levels.

BASIC CIRCUIT SCHEMATIC



NOTE: COMPONENT VALUES ARE TYPICAL.
* ISOLATION DIODE

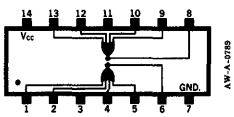
ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 13)

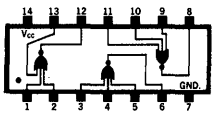
ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS						
		MIN.	TYP.	MAX.	UNITS	TEMP. S8815 S8875 S8885	TEMP. N8815 N8875 N8885	V_{cc}	DRIVEN INPUT	OTHER INPUTS	OUTPUTS	NOTES
A-5	"1" OUTPUT VOLTAGE	2.6			V	-55°C	0°C	4.75V	0.8V	0.8V	-500μA	8
A-3		2.8			V	+25°C	+25°C	5.0V	0.8V	0.8V	-500μA	8
A-4		2.6			V	+125°C	+75°C	4.75V	0.8V	0.8V	-500μA	8
A-5	"0" OUTPUT VOLTAGE			0.4	V	-55°C	0°C	4.75V	2.0V	0V	16mA	9
A-3				0.4	V	+25°C	+25°C	5.0V	2.0V	0V	16mA	9
A-4				0.4	V	+125°C	+75°C	4.75V	2.0V	0V	16mA	9
C-1	"0" INPUT CURRENT	-0.1		-1.6	mA	-55°C	0°C	5.25V	0.4V			
A-3		-0.1		-1.6	mA	+25°C	+25°C	5.25V	0.4V			
C-1		-0.1		-1.6	mA	+125°C	+75°C	5.25V	0.4V			
A-4	"1" INPUT CURRENT			25	μA	+125°C	+75°C	5.0V	4.5V			
A-6	TURN-ON DELAY		8.0	13	ns	+25°C	+25°C	5.0V			D.C.F.O. = 20	10, 14
A-6	TURN-OFF DELAY		10	13	ns	+25°C	+25°C	5.0V			D.C.F.O. = 20	10, 14
C-2	OUTPUT FALL TIME			50	ns	-55°C	0°C	4.75V			A.C.F.O. = 6	11, 14
C-2	INPUT CAPACITANCE			3.0	pf	+25°C	+25°C	5.0V	2.0V			7
A-2	POWER CONSUMPTION (Per Gate)											
	8815 "1"			35.6	mW	+25°C	+25°C	5.25V	0V	0V		
	8875 "1"			27.1	mW	+25°C	+25°C	5.25V	0V	0V		
	8885 "1"			17.8	mW	+25°C	+25°C	5.25V	0V	0V		
	8815 "0"			49.7	mW	+25°C	+25°C	5.25V				
	8875 "0"			43.7	mW	+25°C	+25°C	5.25V				
	8885 "0"			37.3	mW	+25°C	+25°C	5.25V				
C-1	INPUT LATCH VOLTAGE RATING	5.5			V	+25°C	+25°C	5.0V	10mA			12
A-2	OUTPUT SHORT CIRCUIT CURRENT	-20		-70	mA	+25°C	+25°C	5.0V	0V	0V	0V	

NOTES:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1MHz, V_{ac} = 25mV_{rms}. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
8. Output source current is supplied through a resistor to ground.
9. Output sink current is supplied through a resistor to V_{cc}.
10. One DC fan-out is defined as 0.8mA.
11. One AC fan-out is defined as 50pf.
12. This test guarantees operation free of input latch-up over the specified operating supply voltage range.
13. Manufacturer reserves the right to make design and process changes and improvements.
14. Detailed test conditions for AC testing are in Section 3.

8815A A PACKAGE 8875A





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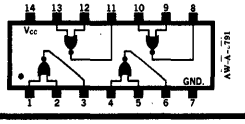

J PACKAGES

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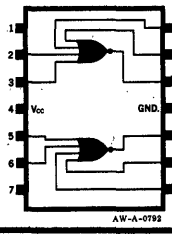

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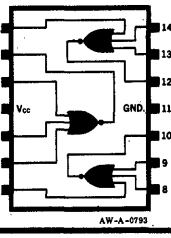
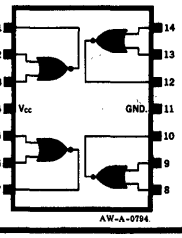


8885J



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